John (Jong Hyun) Kim

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Education

Oregon State University — Corvallis, OR, USA
Ph.D. in Electrical Engineering and Computer Science — *2025 – Present*
- **Advisor:** Prof. Tejasvi Anand
- **Research Focus:** Next-Generation Wireline Transceiver Design.

Konkuk University — Seoul, South Korea
M.S. in Electronic, Information Communication Engineering — *2022 – 2024*
- **Thesis:** "A High-Performance True Random Number Generator for Next-Generation Secure Systems"

Konkuk University — Seoul, South Korea
B.S. in Electrical and Electronics Engineering (Top Honors) — *2016 – 2022*

Technical Skills

Programming & Compute: C++, CUDA, Python, MATLAB, PyTorch, C, Linux, C#, Rust

Hardware Description: Verilog, SystemVerilog

EDA & Simulation Tools: Cadence Virtuoso , Synopsys, Mentor Calibre, KiCad

Core Competencies: SerDes Architecture, EM Simulation, Mixed-Signal IC Design, Hardware Security (TRNG, PUF, FHE)

Research Experience

Oregon State University — Corvallis, OR
Graduate Research Assistant — *Aug 2025 – Present*
- Researching and designing advanced machine learning-based, equalizer-free high-speed interfaces.
- Participated in the Center for Ubiquitous Connectivity (CUbiC) under the DARPA JUMP 2.0 program to advance next-generation interconnect and signaling technologies.

Circuit and System Design Laboratory — Seoul, South Korea
Graduate Student Researcher — *Jan 2020 – Dec 2023*
- [TSMC 28nm] Led chip tape-out for a 40-GS/s, 32-Channel TI-SAR ADC for PAM-4 SerDes Rx (Dec 2022).
- [TSMC 28nm] Led chip tape-out for a 2.5-GS/s pipelined SAR ADC (Jun 2022).
- [Samsung 28nm] Led full-custom SRAM tape-out for high-speed ADCs (Sep 2020).
- [TSMC 28nm] Led chip tape-out for a high-performance true random number generator (TRNG) (Sep 2021). Results published in ASSCC 2022 and JSSC 2024.

Key Projects

MachSpeed: Next-Generation High-Speed SerDes | *SRC / DARPA JUMP 2.0 (CUbiC)* — Aug 2025 – Present
- Researching and developing "MachSpeed," an advanced next-generation high-speed wireline transceiver architecture for future interconnects.
- Designing machine learning-assisted, equalizer-free signaling techniques to optimize power efficiency and signal integrity.
- Conducted under the Center for Ubiquitous Connectivity (CUbiC), supported by SRC and the DARPA JUMP 2.0 initiative.

PIM (Process-In-Memory) Semiconductor Design | *Ministry of Science and ICT* — 2022 – 2023
- Participated in national research center initiatives for next-generation PIM architectures.

Ultra-High Speed Configurable ADC for Beyond-5G | *Ministry of Science and ICT* — 2020 – 2023
- Designed configurable passband ADCs targeting low-power, small-form-factor wireless receivers.

Multi-Band Receiver Architecture for 5G | *Samsung Research Funding* — 2020 – 2022
- Developed bandpass ADC architectures for low-power mobile applications.

Publications

Journal Papers (SCI/SCIE)

- [j4] **Jong Hyun Kim** et al., "A 2.4-Gb/s, 1.9-fJ/bit Nested Chaotic Oscillator-based True Random Number Generator with 4K to 398K Operation", **IEEE Journal of Solid-State Circuits (JSSC)**, 2025. doi:10.1109/JSSC.2025.3602728
- [j3] **Jong Hyun Kim** et al., "A 10-Gb/s True Random Number Generator Using ML-Resistant Middle Square Method", **IEEE Journal of Solid-State Circuits (JSSC)**, 2024. doi:10.1109/JSSC.2023.3346428
- [j2] **Jong Hyun Kim** et al., "An IF Reconfigurable Bandpass Noise-Shaping SAR ADC for IoT and Mobile Application", *Electronics Letters (EL)*, Sep. 2022. doi:10.1049/ell2.12947
- [j1] Kihyun Kim, Jihyun Baek, **Jong Hyun Kim** and Hyungil Chae, "Time-interleaved Noise-shaping SAR ADC based on CIFF Architecture with Redundancy Error Correction Technique", *Journal of Semiconductor Technology and Science (JSTS)*, Oct. 2021.

International Conference Proceedings

- [c3] Hyoungjun Kim, **Jong Hyun Kim**, et al., "A Multispectral Vision Sensor with Embedded Convolutional Neural Network using Programmable Fractional Weights and nMOS-Only PWM Pixels," in **IEEE Symposium on VLSI Circuits**, Kyoto, Japan, June 2025.
- [c2] **Jong Hyun Kim** and Hyungil Chae, "A 10-Gbps, 0.121-pJ/bit, All-Digital True Random-Number Generator Using Middle Square Method", in *Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2022.
- [c1] Jihyun Baek, **Jong Hyun Kim**, Gyuchan Cho, Jintae Kim, and Hyungil Chae, "A 7-Bit 4-GS/s Quad-Channel Time-Interleaved SAR ADC With 2-Then-1-Bit Cycle Conversion," in *Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2022.

Invited Talks

IEEE WMED 2026 Boise, ID, USA
Technical Tutorial: Machine Learning-Based SerDes Equalizer Design *Apr 2026*

Work Experience

ARTEC IT Solutions AG Frankfurt am Main, Hessen, Germany
Full-time R&D Intern *Nov 2018 – Mar 2019*

- Contributed to C# (.NET) development based on the Windows WPF application environment.
- Developed SAP unstructured data archiving systems utilizing SAP Archive Link.
- Managed Microsoft Exchange and Hyper-V based servers.

Fellowships

- Konkuk University, Graduate Fellowship (2022 – 2023)

- Konkuk University, Sang-Huh Undergraduate Fellowship (2016, 2019 – 2021)

References

Prof. Tejasvi Anand
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Email: anandt@oregonstate.edu

Prof. David J. Allstot
Distinguished Special Professor, Electrical and Computer Engineering, Carnegie Mellon University
Email: allstot@andrew.cmu.edu

Prof. Hyungil Chae
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